Attorney's Docket No. 5308-156 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Ryu et al.
Serial No.: To Be Assigned
Filed: Concurrently herewith
For: SILICON CARBIDE POWER METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS HAVING A SHORTING CHANNEL AND METHODS OF FABRICATING SILICON CARBIDE METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS HAVING A SHORTING CHANNEL

Date: July 26, 2001

BOX PATENT APPLICATION
Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Please make the following amendments to the present application prior to examination and prior to calculation of any fees. Applicants provide attached hereto an appendix entitled "VERSION WITH MARKINGS SHOWING CHANGES" showing the changes made by the present Preliminary Amendment.

In the Specification:

Please replace the paragraph beginning at Page 18, line 27 with the following paragraph:

Figure 8F illustrates the formation and patterning of the gate oxide **28**. The gate oxide is preferably thermally grown and is a nitrided oxide. The nitrided oxide may be any suitable gate oxide, however, SiO_2, oxynitride or ONO may be preferred. Formation of the gate oxide or the initial oxide of an ONO gate dielectric is preferably followed by an anneal in N_2O or NO so as to reduce defect density at the SiC/oxide interface. In particular embodiments, the gate oxide is formed either by thermal growth or deposition and then annealed in an N_2O environment at a temperature of greater than about 1100 °C and flow rates of from about 2 to about 8 SLM which may provide initial residence times of the N_2O of from about 11 to about 45 seconds. Such formation and annealing of an oxide layer on silicon carbide are described in commonly assigned United States Patent Application Serial No. 09/834,283, entitled "Method of N_2O Annealing an Oxide Layer on a Silicon Carbide Layer" (Attorney Docket No. 5308-157) or as described in United States Provisional Application Serial